What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An active memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection; and

a circuit coupled between said main memory and said plurality of processing elements, said circuit writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements.

2. The active memory device according to claim 1, wherein said circuit is further adapted to write data from said plurality of processing elements to said memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements.

3. The active memory device according to claim 1, wherein a plurality of processing elements in a first group are coupled to a plurality of data buses of said main memory, each of said plurality of data buses being associated with a respective one of a plurality of addresses in said main memory.

4. The active memory device according to claim 3, wherein said first group includes eight processing elements.

5. The active memory device according to claim 1, wherein said circuit further comprises:

a plurality of circuits, each of said plurality of circuits being associated with a respective one of said plurality of processing elements, each of said plurality of circuits passing data between its associated respective one of said plurality of processing elements and said main memory.

6. The active memory device according to claim 5, wherein each of said plurality of circuits further comprises:

a plurality of logic circuits, each of said plurality of logic circuits having a first input and an output, said first input being coupled to a respective one of a plurality of data buses, each of said plurality of data buses being coupled to said main memory; and

a first multiplexer having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits, and an output coupled to its associated respective one of said plurality of processing elements.

7. The active memory device according to claim 6, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

8. The active memory device according to claim 7, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

9. The active memory device according to claim 6, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

10. The active memory device according to claim 9, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

11. A memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being associated with a respective portion of said main memory, each of said plurality of processing elements having a single bit data output and a single bit data input; and

a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements, each of said plurality of data path circuits having a plurality of inputs, a first input of said plurality of inputs being coupled to said single bit output of a respective one of said plurality of processing elements, at least a second input of said plurality of inputs being coupled to a respective one of a plurality of data buses of said main memory, and an output coupled to said single bit input of a respective one of said plurality of processing elements,

wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in

said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time.

12. The memory device according to claim 11, wherein each of said data path circuits is further adapted to write data from said plurality of processing elements to said main memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements.

13. The memory device according to claim 11, wherein each of said plurality of data path circuits further comprises:

a plurality of logic circuits, each of said plurality of logic circuits having a first input and an output, said first input being coupled to said at least a second input of said plurality of inputs of said data path circuit; and

a first multiplexer having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits, and an output coupled to said output of said data path circuit.

14. The memory device according to claim 13, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

15. The memory device according to claim 14, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

16. The memory device according to claim 13, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

17. The memory device according to claim 16, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

18. A circuit for connecting a memory device and a processing element of an active memory comprising:

a first multiplexer having a first input coupled to said processing element and a second input coupled to a data bus of said memory device;

a first register having an input and an output, said input being coupled to an output of said first multiplexer;

a second multiplexer having an input coupled to said output of said first register and an output coupled to said processing element;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said data bus; and

a second tri-state device having an input coupled to said output of said first register and an output coupled to said data bus and a third input of said first multiplexer.

19. The circuit according to claim 18, wherein said output of said second tri-sate device is coupled to a different data bus than said output of said first tri-state device.

20. The circuit according to claim 18, further comprising:

a second register having an input coupled to said output of said first multiplexer;

a third multiplexer having a first input, a second input, and an output, said first input being connected to an output of said second register, said output from said first register being coupled to said second input, said output being coupled to said input of said second multiplexer; and

a fourth multiplexer having a first input, a second input, and an output, said first input being coupled to said output of said first register, said second input being coupled to said output of said second register, said output being coupled to said input of said first and second tri-state devices.

21. The circuit according to claim 20, wherein said output of said second tri-sate device is coupled to a different data bus than said output of said first tri-state device.

22. A processing system comprising:

a processing unit; and

an active memory device coupled to said processing unit, said active memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection; and

a circuit coupled between said main memory and said plurality of processing elements, said circuit writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said

main memory in a horizontal mode from said main memory to said plurality of processing elements.

23. The processing system according to claim 22, wherein said circuit is further adapted to write data from said plurality of processing elements to said memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements.

24. The processing system according to claim 22, wherein a plurality of processing elements in a first group are coupled to a plurality of data buses of said main memory, each of said plurality of data buses being associated with a respective one of a plurality of addresses in said main memory.

25. The processing system according to claim 24, wherein said first group includes eight processing elements.

26. The processing system according to claim 22, wherein said circuit further comprises:

a plurality of circuits, each of said plurality of circuits being associated with a respective one of said plurality of processing elements, each of said plurality of circuits passing data between its associated respective one of said plurality of processing elements and said main memory.

27. The processing system according to claim 26, wherein each of said plurality of circuits further comprises:

a plurality of logic circuits, each of said plurality of logic circuits having a first input and an output, said first input being coupled to a respective one of a plurality of data buses, each of said plurality of data buses being coupled to said main memory; and

a first multiplexer having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits, and an output coupled to its associated respective one of said plurality of processing elements.

28. The processing system according to claim 27, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

29. The processing system according to claim 28, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

30. The processing system according to claim 27, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

31. The processing system according to claim 30, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

32. The processing system according to claim 22, wherein said processing unit and said active memory device are on a same chip.

33. A processing system comprising:

a processing unit; and

a memory device coupled to said processing unit, said memory device comprising:

a main memory;

a plurality of processing elements, each of said plurality of processing elements being associated with a respective portion of said main memory, each of said plurality of processing elements having a single bit data output and a single bit data input; and

a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements, each of said plurality of data path circuits having a plurality of inputs, a first input of said plurality of inputs being coupled to said single bit output of a respective one of said plurality of processing elements, at least a second input of said plurality of inputs being coupled to a respective one of a plurality of data buses of said main memory, and an output coupled to said single bit input of a respective one of said plurality of processing elements,

wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time.

34. The processing system according to claim 33, wherein each of said data path circuits is further adapted to write data from said plurality of processing

elements to said main memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements.

35. The processing system according to claim 33, wherein each of said plurality of data path circuits further comprises:

a plurality of logic circuits, each of said plurality of logic circuits having a first input and an output, said first input being coupled to said at least a second input of said plurality of inputs of said data path circuit; and

a first multiplexer having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits, and an output coupled to said output of said data path circuit.

36. The processing system according to claim 35, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

37. The processing system according to claim 36, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

38. The processing system according to claim 35, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

39. The processing system according to claim 38, wherein said output of said second tri-state device is coupled to said respective one of said plurality of data buses.

40. The processing system according to claim 33, wherein said processing unit and said memory device are on a same chip.

41. A method for writing data from a processing element to a memory device comprising the steps of:

providing a plurality of data bits in a serial manner from said processing element to a data circuit;

passing said data through said data circuit; and

writing said data to said memory device,

wherein said data circuit passes said data directly to said memory device in a horizontal mode.

42. The method according to claim 41, wherein said step of passing said data further comprises:

outputting each bit of said plurality of data bits from said data circuit on a different data bus associated with said memory device; and

wherein said step of writing said data further comprises writing said each bit of said plurality of bits data bits to a location in said memory device associated with a different address.

43. The method according to claim 42, wherein said step outputting further comprises:

passing each bit of said plurality of data bits through a respective register.

44. The method according to claim 42, wherein each different memory address has an associated plurality of bits, and wherein said step of writing each said data bit further comprises:

writing said each bit into a same bit of said associated plurality of bits in each said different memory address.

45. The method according to claim 41, wherein said circuit is further adapted to pass at least a portion of said data to said memory device in a vertical mode.

46. The method according to claim 45, wherein said step of passing said at least a portion of said data further comprises:

outputting each bit of said plurality of data bits from said data circuit on a different data line of a single data bus associated with said memory device; and

wherein said step of writing said data further comprises writing said each bit of said plurality of bits data bits to successive bit locations associated with a single address.

47. The method according to claim 46, wherein said step outputting further comprises:

passing each bit of said plurality of data bits through a respective register.

48. A method for reading data stored in a memory device and providing said data to a processing element, said method comprising the steps of:

providing a plurality of data bits from said memory device to a data circuit;

passing said data through said data circuit; and

outputting said data to said processing element in a serial manner,

wherein said data is stored in said memory device in a horizontal mode.

49. The method according to claim 48, wherein said step of passing said data further comprises:

passing each bit of data associated with a single address through a respective register; and

inputting said each bit of data associated with said single address to a multiplexer,

wherein said multiplexer outputs said each bit of data in a serial manner to said processing element.

50. The method according to claim 48, wherein at least a portion of said data is stored in said memory device in a vertical mode.

51. The method according to claim 50, wherein said step of passing said at least a portion of said data further comprises:

passing a respective bit of data associated with a different address through a respective register; and

inputting each said respective bit of data associated with said different address to a multiplexer,

wherein said multiplexer outputs said each said respective bit of data in a serial manner to said processing element.